UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,431	04/09/2004	Robert E. Cypher	5181-96100	1240

35690 7590 11/09/2006

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
700 LAVACA, SUITE 800
AUSTIN, TX 78701

EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,431	CYPHER ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-11, 13-17, 19-24, 26-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-11,13-17,19-24,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
11/7/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgment is made of the amendments to the claims and title.

2. Objection to the title is withdrawn after considering amendments.

Response to Arguments

3. Applicant's arguments filed 14 August 2006 have been fully considered but they are not persuasive.

Examiner notes that oath does include City and State of Residence of Stevan Vlaovic; and even though the form was not completed fully, information can be ascertained without having to refer to other documents and therefore the objection to the oath is withdrawn.

Applicant argues, "The Examiner asserts that Loh teaches a first storage and a second storage (elements 405) and that 'the global history could be used to index the predictors.' Applicant can find no such teaching in Loh... Loh does not disclose the generation of 'a first index for accessing a selected location within said first storage' and the generation of 'a second index for accessing a selected location within said second storage,' as recited in claim 1."

The branch predictors 405 of figure 4 are connected to segments of a prediction history register, which are storage elements.

It is noted that the rejection is not meant to mean Loh teaches indices but rather the combination of Loh and McFarling teaches indices. The rejection was meant to be a combination of Loh and McFarling. It is stated that Loh does not teach such disclosure and the McFarling does. The rejection is clarified below.

Applicant argues, "McFarling does not disclose 'performing a first hash function on input branch information to generate a first index for accessing a selected location within said first storage and performing a second hash function on said input branch information to generate a second index for accessing a selected location within said second storage.' "

Examiner would like to note that McFarling paragraph 26, lines 10-13 refer to the case of just performing one hash function; however, in figure 14 and paragraphs 87-89 refers to the case of performing multiple hash functions in which multiple storages can be accessed.

In regards to claims 8 and 11, Applicant correctly points out that Loh does not teach using saturating counters. A typographical error was made and it was meant to say McFarling teaches saturating counters. Such disclosure can be found in paragraph 53 of McFarling, which teaches two-bit saturating counters (i.e. it can count from 0-3).

Claims 6 and 19 are addressed below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 6 and 19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

It is unclear as to where in the Specification the newly amended limitations of a "different subset of bits" are disclosed. The Remarks submitted do not point to where in the Specification such disclosure can be found, and the Examiner could not find support of such disclosure in the Specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 6-8, 13-17, 19-20, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loh (US Pat. Appl. Pub. 2005/0223203; herein referred to as "Loh".) in view of McFarling (US Pat. Appl. Pub. 2001/0056531; herein referred to as "McFarling".).

Regarding **independent claim 1**, Loh discloses *a branch prediction mechanism comprising: a first storage including a first plurality of locations for storing a first set of partial prediction information* [see Loh, Fig. 4, element 405 (e.g., "Branch Predictor 1")]*; a second storage including a second plurality of locations for storing a second set of partial prediction information* [see Loh, Fig. 4, element 405 (e.g., "Branch Predictor 2"); Examiner's note: Loh does not limit the invention to a particular type of predictor, however, McFarling states that global history could be used to index the predictors, thus it is inherent that global predictors would be utilized as the predictors. An example of a common global predictor is shown in McFarling, Fig. 4. N.B., a global predictor contains an array of saturating counters.]*; wherein said control unit is further configured to provide a prediction value based on corresponding partial prediction information in said selected locations of said first and said second storages* [see Loh, Fig. 4, element 410; Para 0020, lines 3-7; Examiner's note: Since Loh discloses the prediction of segments of a branch history, it is clear that the intermediate predictions are for the segments and thus are only partial predictions, thus the need for a mechanism to determine a final prediction which is disclosed by Loh in element 410 of Figure 4.].

Loh does not disclose *performing a first hash function on input branch information to generate a first index for accessing a selected location within said first storage and* performing *a second hash function on said input branch information to generate a second index for accessing a selected location within said second storage wherein said input branch information includes address information corresponding to a fetch address of a current branch instruction or control unit further configured to update said selected locations of said first and said second storages dependent on whether said prediction value yields an accurate branch prediction.*

McFarling does disclose *performing a first hash function on input branch information to generate a first index for accessing a selected location within said first storage and* performing *a second hash function on said input branch information to generate a second index for accessing a selected location within said second storage* [see McFarling, Para. 0026, lines 10-13 and Figure 14 and Para. 0087-0089; Examiner's note: McFarling discloses utilizing a hashing function to index global predictors. And the case of performing multiple hash functions in which multiple storages can be accessed is shown], *wherein said input branch information* [including] *address information corresponding to a fetch address of a current branch instruction* [see McFarling, Fig. 5, element 50; Para. 0026, lines 10-13 "...the branch instruction address...".]. McFarling also discloses a *control unit...further configured to update said selected locations of said first and said second storages dependent on whether said prediction value yields an accurate branch prediction* [see McFarling, Para. 0021, lines 6-9; Examiner's note: McFarling discloses tracking branch instructions which would

involve updating the counters in a branch predictor. Furthermore, the primary goal of a branch predictor employing saturating counters, such as the well known counters proposed by Lee and Smith, would have been to update said counters based on branch execution.].

The advantage of using a hash function to index a global predictor would have been to improve the global prediction accuracy [see McFarling, Para. 0026, lines 13-15]. This advantage is desirable in the environment disclosed by Loh as improving the accuracy of a branch prediction would increase the performance of an entire processor by reducing the amount of mispredictions and in turn fetching errors. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize a hashing mechanism, as disclosed by McFarling, to index a set of predictors as disclosed by Loh. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a hashing mechanism to index a set of predictors with the goal of increasing prediction accuracy.

Regarding **claim 2**, Loh discloses the *prediction value* [providing] *a strongly/weakly taken/not taken branch prediction indication that is indicative of whether the current branch instruction is taken upon execution* [see Loh, Para. 0020, lines 3-7; Examiner's note: Loh discloses a final prediction being a function of the partial predictions, if said partial predictions are based on a commonly used n-bit saturating counter (commonly known at the time of invention), it is inherent that the final prediction based on said partial predictions would have been of the same format.].

Regarding **claim 3**, Loh discloses said input branch information [including] branch history information corresponding to an outcome of a number of preceding branch instructions [see Loh, Para. 0021].

Regarding **claim 4**, Loh discloses *said first hash function and said second hash function...configured to operate on a portion of said branch history information* [see Loh, Para. 0018, lines 9-11].

Claim 5 has been cancelled.

Regarding **claim 6**, Loh discloses said first hash function and said second hash function...configured to operate on a different subset of bits of said fetch address [see Loh, Para. 0018, lines 9-11 and figure 4: Loh teaches "The prediction history information may be accessed in segments by a number of intermediate branch prediction units 405" and it is shown in figure 4 that these segments are non overlapping and thus would be of a different subset of bits].

Regarding **claim 7**, Loh discloses *each of said first and said second sets of partial prediction information* [including] *a plurality of counter values each corresponding to a strongly/weakly taken/not taken branch prediction indication that is indicative of whether the current branch instruction is taken upon execution* [see Loh, Para. 0020,

lines 3-7; Examiner's note: Loh discloses a final prediction being a function of the partial predictions, if said partial predictions are based on a commonly used n-bit saturating counter (commonly known at the time of invention), it is inherent that the final prediction based on said partial predictions would have been of the same format.].

Regarding **claim 8**, Loh and McFarling do not explicitly disclose the *control unit* [being] *further configured to use said prediction value to determine whether the current branch instruction is taken upon execution, wherein said prediction value is generated by summing respective counter values stored within said selected location within said first storage and said selected location within said second storage.*

However, McFarling discloses using multiple values of saturating counters (typically ranging between the value of 0-3 as common at the time) and performing an action on said counters to derive a final prediction. At the time of invention it would have been obvious that an addition or average (inherently containing addition) of the partial counter values would have resulted in the best prediction with the least amount of overhead.

Claim 12 has been cancelled.

Regarding **claim 13**, Loh discloses *a third storage including a third plurality of locations for storing a third set of partial prediction information and wherein said control unit is further configured to perform a third hash function on said input branch*

information to generate a third index for accessing a selected location within said third storage [see Loh, Fig. 4, element 405 (e.g., "Branch Predictor *k*"); Examiner's note: Loh does not place a limit on how many intermediate predictors are possible in the invention.].

Claims 14-17, 19-21, and 26 are rejected as being the method performed by the apparatus in claims 1-4, 6-8, and 14, respectively.

Claims 18 and 25 have been cancelled.

Claim 27 is rejected as being the branch prediction mechanism performed by the apparatus in claim 1.

6. Claims 9-11 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loh in view of McFarling, further in view of Yeh et al. (US Pat. No. 6,427,206; herein referred to as "Yeh".).

Regarding **claim 9**, Loh, McFarling and Yeh disclose the limitations as stated in **claim 9**.

Yeh further discloses *each of said first and said second sets of partial prediction information* [including] *a plurality of counter values each corresponding to a strongly/weakly agree/disagree indication that is indicative of whether said branch*

prediction hint bit embedded within said current branch instruction is to be used by said control unit [see Yeh, Col. 6, lines 18-35; Examiner's note: Yeh discloses using a hardware branch predictor if confidence in the compiler hint is not strong, that is, if the compiler is below a threshold of assuredness a branch prediction is further utilized to determine whether the hint bit is correct (e.g., hint = taken, predictor = strongly taken) or if the bit is incorrect (e.g., hint = taken, predictor = strongly not-taken).].

The advantage of utilizing a hint bit in conjunction with a branch prediction scheme would have been to determine in advance how certain a processor will be on the taken/not-taken tendencies of a branch instruction prior to its execution based on profiling the instruction by a compiler (Col. 2, lines 5-7). This advantage would have been desirable in the invention of Loh and McFarling as it would have sped up execution for branches that have been profiled correctly as strongly taken or strongly not-taken. Furthermore, as admitted by the applicant, modern processors are known to support a hint bit encoded by the compiler, therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to account for the hint bit in modern processors in the invention of Loh and McFarling. This advantage would have motivated one of ordinary skill in the art at the time of invention to account for the prediction hint and allow a branch prediction unit to use the hint to its advantage in determining the correct path of a branch.

Regarding **claim 10**, Loh and McFarling disclose the limitations as stated in **independent claim 1**.

Loh and McFarling do not disclose *the control unit is further* [being] *configured to use said prediction value to control whether a branch prediction is performed in accordance with a branch prediction hint encoded within a current branch instruction.*

Yeh does disclose *the control unit is further* [being] *configured to use said prediction value to control whether a branch prediction is performed in accordance with a branch prediction hint encoded within a current branch instruction* [see Yeh, Col. 6, lines 18-35; Examiner's note: Yeh discloses the use of a prediction "hint" (Col. 2, lines 62-64) encoded into the instruction by the compiler. This hint is utilized in conjunction with a branch prediction scheme (Col. 6, lines 18-35) to determine the appropriate branching behavior.].

The advantage of utilizing a hint bit in conjunction with a branch prediction scheme would have been to determine in advance how certain a processor will be on the taken/not-taken tendencies of a branch instruction prior to its execution based on profiling the instruction by a compiler (Col. 2, lines 5-7). This advantage would have been desirable in the invention of Loh and McFarling as it would have sped up execution for branches that have been profiled correctly as strongly taken or strongly not-taken. Furthermore, as admitted by the applicant, modern processors are known to support a hint bit encoded by the compiler, therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to account for the hint bit in modern processors in the invention of Loh and McFarling. This advantage would have motivated one of ordinary skill in the art at the time of invention to account for the

prediction hint and allow a branch prediction unit to use the hint to its advantage in determining the correct path of a branch.

Regarding **claim 11**, Loh, McFarling, and Yeh disclose the limitations as stated in **claim 10**.

Loh, McFarling, and Yeh do not explicitly disclose *the prediction value* [being] *generated by summing respective counter values stored within said selected location within said first storage and said selected location within said second storage.*

However, McFarling discloses using multiple values of saturating counters (typically ranging between the value of 0-3 as common at the time) and performing an action on said counters to derive a final prediction. At the time of invention it would have been obvious that an addition or average (inherently containing addition) of the partial counter values would have resulted in the best prediction with the least amount of overhead.

Claims 22-24 are rejected as being the method performed by the branch prediction mechanism in claims 9-11, respectively.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Lai
Examiner
Art Unit 2181

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
11/7/2006

vl
November 3, 2006